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ADC Techniques for Optimized Conversion Time in CMOS Image Sensors

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***Abstract* – For several decades, many CMOS Image Sensors (CIS) with a small pixel size have used single slope column parallel ADCs (SS-ADC). It is well known that the main drawback of this ADC is the conversion speed. This paper presents several ADC architectures which improve the speed of a SS-ADC. Different architectures are compared in terms of ADC resolution, power consumption, noise and conversion time.**

Keywords – CMOS image sensor, Piece-wise-linear ramp, Photon shot noise, Calibration.

I. INTRODUCTION

Before the advent of CMOS image sensors, CCD sensors were used with signal conversion taking place off the sensor. With CMOS sensors, ADCs are embedded in the sensor. Since the capacitance of an on-chip ADC is smaller than that of an external ADC, faster settling times and, thus, faster conversion rates are possible. As shown in Figure 1, several architectural possibilities for embedding the ADC have been considered.

The first ADC embedded on a CMOS sensor was a Successive Approximation Register (SAR) ADC [1], as shown in Figure 1.A. This sensor is fast although the readout process is still sequential. In order to increase the readout speed, the architecture of CMOS image sensors moved to column parallel ADCs [2]. Indeed this technique involves parallelizing the digital part, but constraints the area of the ADC to be within the pitch of one column, as shown in Figure 1.B. To alleviate this problem, one can split the readout architecture into top and bottom readouts at twice the column pitch, or one can keep the same pitch and increase the number of ADCs to increase the speed of conversion. For improving Signal-to-Noise Ratio (SNR), the converter can also be implemented inside the pixel, as in Figure 1.C. This results in a faster conversion since the parasitic load of other pixels and the column are largely reduced, but it reduces the fill factor. In this case the ADC must be simple, small and low power.

For all these reasons, the best solution for a CMOS image sensor with a small pixel size has been to parallelize the ADC into each column. However, ADC parallelization does not always provide the required speed conversion as the size of the pixel array continues to increase along with a demand for higher frame rate. Enhanced architectures that allow for higher frame rates are required. Several works on this topic have targeted a speed increase using successive approximation register [3], cyclic [4], and single ramp [5] ADCs. The latter is the most commonly used since it is small and easily compatible with the architecture of one ADC per column.

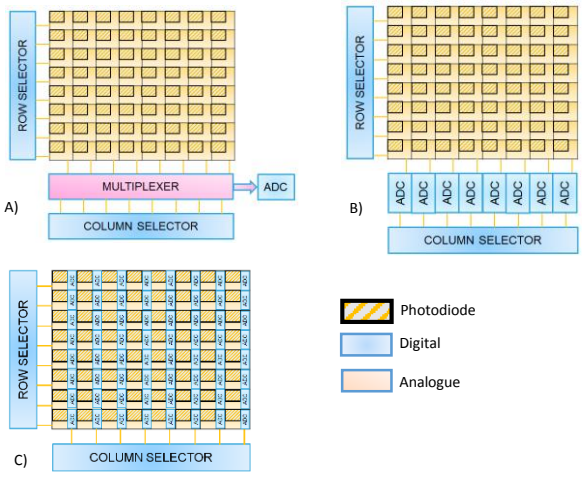

Figure 1: Several architectures to increase readout speed.

However, the main drawback of this architecture is the conversion time because 2^N clock cycles are required to perform the conversion instead of N cycles for SAR or cyclic ADCs.

One technique for significantly increasing the speed of the conversion exploits the fact that the photon shot noise does not affect equally all signal levels. This noise is due to the discrete nature of the photons themselves. The random arrivals of photons on the CMOS sensor can thus be described by Poisson statistics. This means that for a number of photons equal to $N_{ph,}$ the associated noise σ_{ph} is given by:

$$\sigma_{ph} = \sqrt{N_{ph}} \qquad [1]$$

The ADC quantization noise is equal to:

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$$\sigma_{ADC} = \frac{V_{LSB}}{\sqrt{12}} \quad [2]$$

As the number of photons increases, the quantization noise does not need to be kept as low as for a smaller signal. For example, it is possible to increase the LSB of the ADC by simply increasing the slope of the ramp. We have considered this for the different ADC architectures studied.

This paper is organised as follows. In section II, the single slope ADC will be described. Next, we compare several techniques which adapt the slope to the level of photon shot noise (or to the signal level). Multiple Ramp Multiple Slope (MRMS), Piece-Wise-Linear ramp (PWL) and continuous non-linear test techniques are presented in Section III-V, respectively. Finally, Section VI concludes the paper.

II. SINGLE SLOPE ADC ARCHITECTURE

The SS-ADC is composed of three parts: a ramp generator, a comparator and a counter. A typical architecture of a single slope ADC is shown on Figure 2.

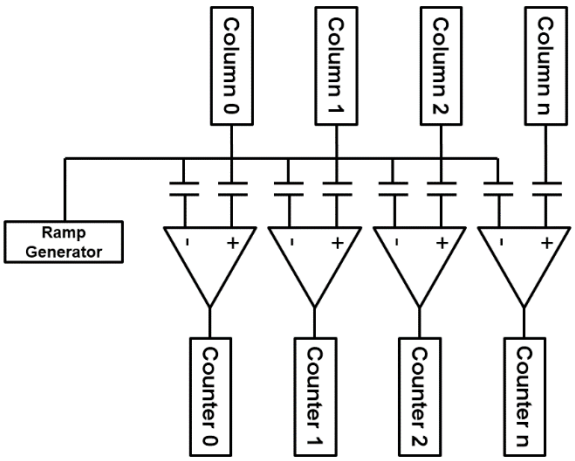

Figure 2: Column parallel SS-ADC architecture.

The conversion is very simple, the analogue pixel value is compared to an analogue ramp. The counter stops counting when the pixel value is equal to the ramp value. Then the value in the counter becomes the converted value.

The ADC is a critical block of the sensor, being the bottleneck to increase the frame rate. It can also be responsible for increased noise. Indeed, Vertical Fixed Pattern Noise (VFPN) and line noise mostly depend on the ADC design. The VFPN is due to the column-to-column mismatch of the comparator. To remove this noise, Digital Correlated Double Sampling (D-CDS) allows best-in class VFPN as mentioned in [6]**.** The D-CDS consists in performing the conversion twice: once for the reference level of the pixel (or reset level) and once for the pixel signal level. As for the line noise, it is commonly due to the Power Supply Rejection Ratio (PSRR) of the ramp generator because it is globally distributed to all comparators. To make the line noise invisible to the human eye, it is demonstrated that it should be at least ten times smaller than the read noise as explained in [7]. In spite of that, the ramp generator is a good candidate for improving the conversion time because, as we will see afterwards, it is on this block that we can adapt to the photon shot noise.

Another solution is to speed up the counter [8] but there are limitations of increasing the clock frequency of the ripple counter in the case of a linear ramp ADC: power consumption is increased, while a shorter LSB in the time domain brings a requirement for better noise performance. Actually it is a trade-off between power consumption and speed.

III. MULTIPLE RAMP MULTIPLE SLOPE

The MRMS is a technique involving a coarse conversion and a fine conversion. Usually a SS-ADC requires 2^n comparisons for an 'n' bit. In [9], a mix between SS-ADC and SAR ADC is proposed for an ADC that is composed of two conversions. The first one divides in 'm' steps the dynamic range to find a good starting point for the fine conversion, which implies a feedback between the comparator and the reference generator as one can see below. In the coarse phase, all columns are shorted to the coarse ramp generator and results are stored in a memory distributed in each column. All results of this conversion are then used to control a switch to connect the right slope to the right column. The architecture of this ADC is shown in Figure 3 and the timing diagram of Figure 4.

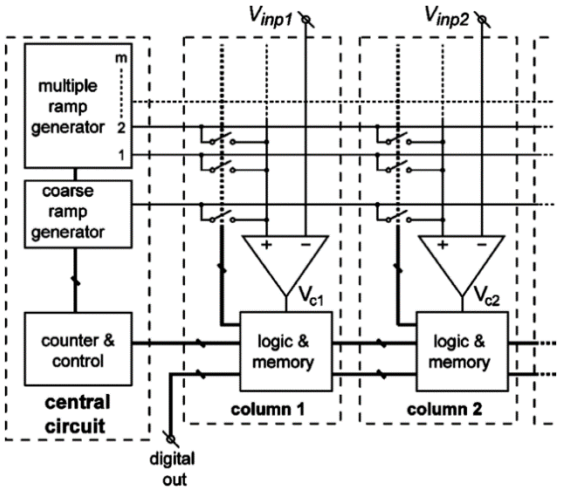

Figure 3: Architecture of the MRMS technique.

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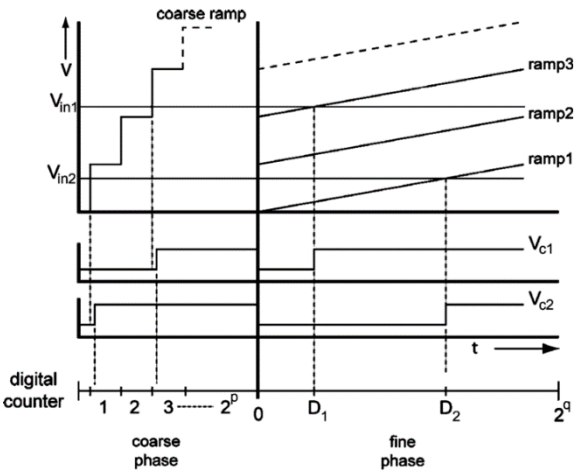

Figure 4: Timing for the Multiple Ramp Single Slope ADC.

By using 8 ramps, this architecture reduces the conversion time by 3.3 times but the power consumption is increased by 16%. This result is acceptable since the Figure of Merit is improved. Unfortunately, the area increases as well because of the additional memory in each column. To adapt to the photon shot noise, the quantization step in the coarse conversion must be varied along with the dynamic range. In this case, the dynamic range is covered faster as shown in Figure 5.

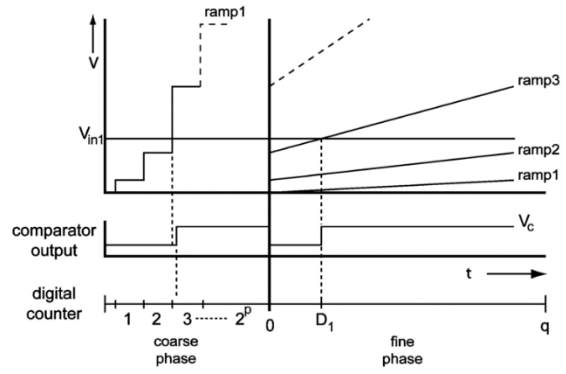

Figure 5: Timing for the Multiple Ramp Multiple Slope ADC.

With this technique the conversion time is reduced by about 25%, without an increase in the power consumption or the area, because only reference voltages change. This is important for resolutions above 10 bits.

IV. PIECE-WISE-LINEAR RAMP

In this work, a readout architecture has been developed to read a 13Mpix sensor (4248 x 3216) at 55 frames/s, requiring a row time of 5.5µs. Figure 6 shows a block diagram of the sensor. The readout circuits use a digital CDS (D-CDS) that allows for Vertical Fixed Pattern Noise (VFPN) free of mismatch. A 10b column-parallel ADC includes an integration capacitance which is a part of the PWL ramp generator, a buffer, a comparator and a ripple counter. And, finally, a compiled digital calibration algorithm on the right side allows the calibration of the converted data. The ADC is located on the top and bottom of the pixel array that allow a layout pitch for the readout circuits of 2.2µm, which is twice the pixel pitch.

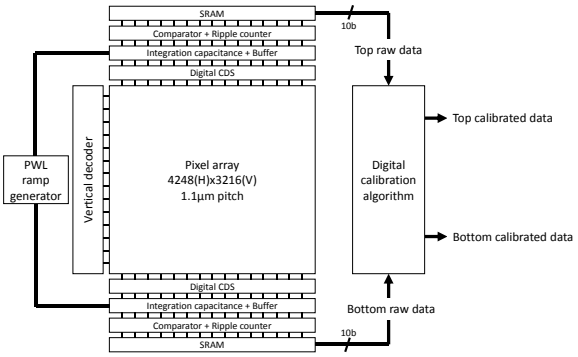

Figure 6: Block diagram

Figure 7 shows a simplified schematic diagram of the PWL ramp generator. It is based on a switched current source with an integration capacitance. The variable current source is composed to an array of 11b thermometric unit elements and an integration capacitance distributed in column. Among the 11b input data, 8b are dedicated to control the analogue gain from 0.25 to 16. Three additional bits are employed to fine trimming for lot-to-lot mismatch of the fringe capacitances and the mismatch of the integration current. The use of a buffer prevents smearing issues caused by a ramp distortion when many comparators simultaneously change state.

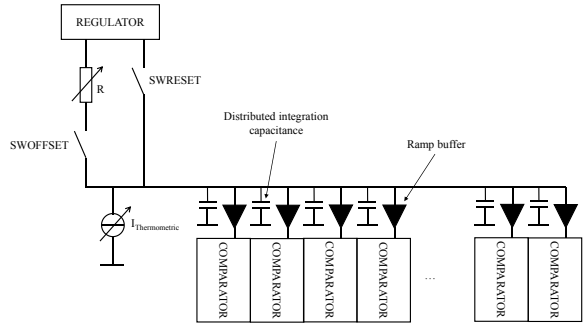

Figure 7: Schematic of the I/C ramp generator.

In typical case, this ramp generator allows generating a slew rate in the range of 30 mV/µs – 0.5 V/µs with 1 mV/µs step. Figure 8 shows a timing diagram of one readout period. The period is 5.5µs at a frame rate of 55fps with 3216 rows. To ease the linearization process, the ramp ratio between two consecutive segments is designed to be a power of 2. Compared to a "usual" ramp generator, the PWL ramp

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shows the same power consumption and the same area. With only two segments, the conversion time can be reduced by 25%. The switches SWOFFSET and SWRESET allow, respectively, the generation of an offset before starting the ramp and the reset of the integration capacitance. Due to non-correlated kTC noise sources occurring during the reset phases, the integration capacitance has to be large enough to prevent a drop of the line noise performance. Furthermore, since the two reset phases are uncorrelated, the regulator on Figure 7 which generates the reference reset voltage needs to have 63dB of Power Supply Rejection Ratio (PSRR) above 100 KHz to reduce line noise below 15µV RMS.

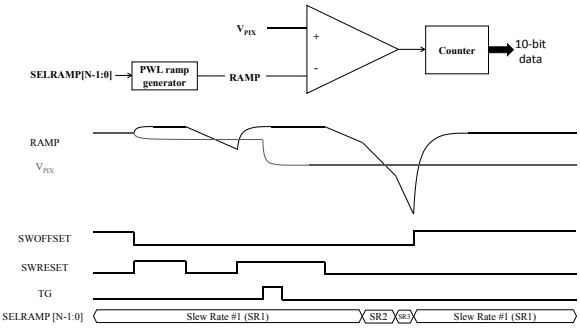

Figure 8: Timing diagram of the Piece wise linear ramp generator

However, the drawback of this architecture is the need of calibration, as the comparator delay is modulated with the slope of the ramp. However D-CDS allows compensating only one segment of the PWL ramp. As shown in Figure 9, D-CDS accurately linearizes the first segment corresponding to low light conditions. Nevertheless high distortion occurs at the knee points and processing is required to compensate it.

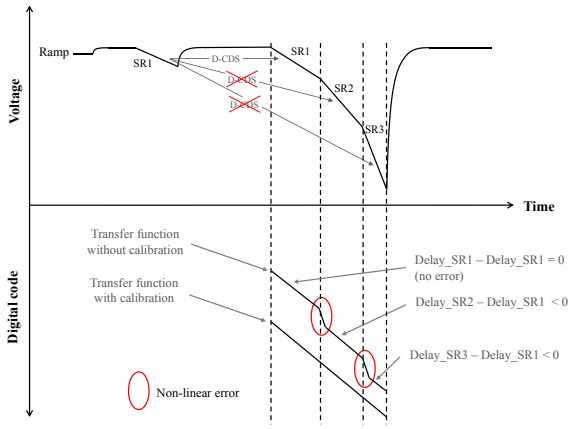

Figure 9: Conversion errors introduced during the conversion.

The design is more complex due to the calibration techniques but it results in +/-0.5 LSB of DNL as can be seen in Figure 10.

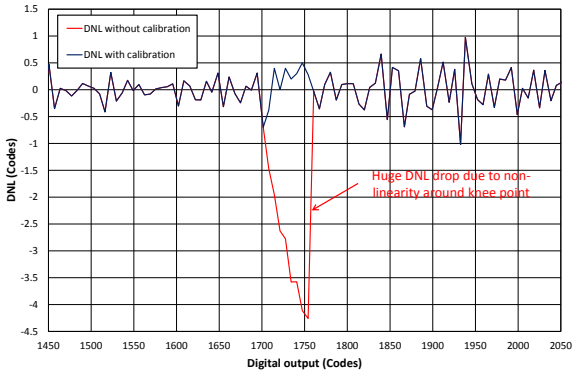

Figure 10: DNL before and after calibration.

The prototype image sensor has been fabricated in a 65nm 1P5M CIS process. The die size is 6.5mm(V)x6.3mm(H). The PWL ramp generator is placed on the left side at the exact middle of the array to get the same wiring length of the data transfer path to avoid differences between the readout on top and bottom sides. Figure 11 shows the die micrograph of the fabricated sensor.

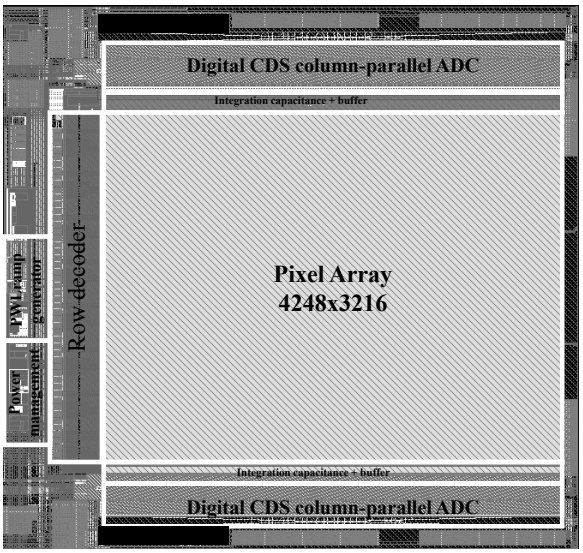

Figure 11 : Chip Micrograph

V. CONTINUOUS NON-LINEAR INPUT

Another way to increase the frame rate of the sensor consists in using a continuous nonlinear input. As explained before, the ramp step can be increased for a strong signal because the quantization noise is overcome by the photon shot noise. The main advantage is that there is no knee point, so the modification of gain is smoother and there is no missing code, even without calibration, as opposed to the previous method. [10] describes one way to

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generate this kind of ramp and the schematic can be seen in Figure 12. Indeed, by integrating a time dependent current we get a quadratic equation that realizes the waveform as shown in Figure 10.

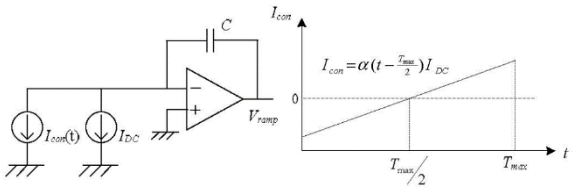

Figure 12: schematic of a nonlinear ramp.

In [11], an imager of 2352x1728 pixel array with 12-bit column-parallel ADCs ramp has been developed. In this case, the row conversion time must be longer than 4095 clock cycles. However, to avoid some artifacts, a parameter called shot noise margin is introduced.

12-bit Ramp Cycles and M_{shot} at N_{sat} = 20ke$^-$

Mode	Linear	0dB	-6dB	-12dB
Ramp Steps	4095	298	607	1240

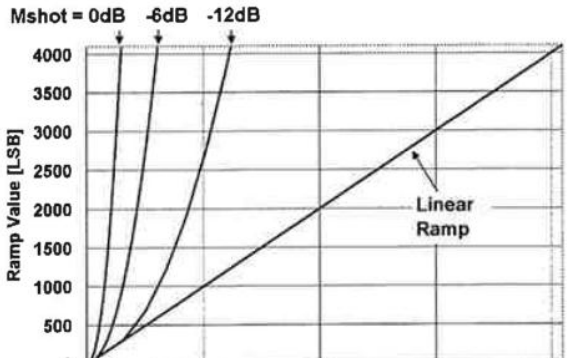

Figure 13: Timing of the nonlinear ramp for different margin [11].

As can be seen in Figure 13, with 0dB of margin it is possible to do the conversion within only 298 clock cycles, leading to a reduction of the conversion time by almost 14.

But the most difficult part of this structure is for re-linearization of the output, as an exponential counter is required. This will lead to area and power consumption increase. Finally the counter must remain synchronized with the ramp, which is challenging due to the time propagation along the array. Besides, the best technique to reach a good VFPN is to use D-CDS, although it is more complex in this case because we subtract a value for the reset signal which has been converted with a nonlinear input.

VI. CONCLUSION

A 13Mpix BSI CMOS image sensor implementing a PWL ramp generator based on an I/C structure has been developed. 5.5µs row time has been reached with DNL results after calibration exhibiting +/-0.5 LSB. Table 1 shows a comparison of performances between several state-of-the-art techniques. The Analogue CDS (A-CDS) approach is more sensitive to FPN but the MRMS method demonstrates faster conversion as well as more complexity due to the larger number of ramps generated. [12] reduces drastically the VFPN with Hybrid-CDS (H-CDS) compared to the A-CDS but increases the conversion time due to more conversion within same row period. Finally, the idea in [8] is to speed up the ripple counter to reduce the line period, to the detriment of power consumption.

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Table 1: Comparison and measured performance.

	[8]	[9]	[11]	[12]	This work
ADC type	SS	MRMS	Nonlinear Ramp	SS	PWL Ramp
ADC Resolution (bits)	12	5b-coarse / 6b-fine	12	10	10
Pixel Resolution (Mpix)	17.7	320x240	2352x1728	320x240	13
Pixel pitch (µm)	4.2	5.6	2.9	2.25	1.1
Row Line time (µs)	7.4	4.5	11.9**	29	5.5
Column FPN (LSB)	2.64*	4.16	5 (average)	0.8	0.03
CDS Type	D-CDS	A-CDS	A-CDS	H-CDS	D-CDS
Power consumption per column	366 µW	150 µW	N/A	109 µW	25µW

** w/o additional correction circuit.*
***24MHz of ramp clock.*

VII. REFERENCES

[1] Z. Zhou *et al*., "CMOS Active Pixel Sensor with On-Chip Successive Approximation Analog-To-Digital Converter," IEEE Transactions on Electron Devices, vol. 44, n°1044 (1997), 1759–1763.

[2] A.I. Krymski *et al*., "A High-Speed, 240-Frames/s, 4.1-Mpixel CMOS Sensor," IEEE Transactions on Electron Devices, 50 (2003), 130–135.

[3] S. Matsuo *et al.* , "8.9-Megapixel Video Image Sensor With 14-b Column-Parallel SA-ADC," IEEE Transactions on Electron Devices, vol. 56 (2009), 2380–2389.

[4] K. Kitamura, *et al*., Column-parallel Pipelined Cyclic Adcs, "A 33Mpixel 120fps CMOS Image Sensor Using 12b Column-Parallel Pipelined Cyclic ADCs," IEEE International Solid-State Circuits Conference, (2012), 388–390.

[5] A. Theuwissen, "CMOS Image Sensors : State-Of-The-Art and Future Perspectives", IEEE, 2007, 21–27.

[6] S. Kuramochi, et al., "A 1/1.8-inch 6.4MPixel 60 frames/s CMOS Image Sensor With Seamless Mode Change," IEEE Journal of solid-state circuits vol. 41, n°12, p2998–3006, 2006.

[7] R. Baer, "Noise at the system level," in IEEE ISSCC 2007 short course – Noise in imaging systems, Feb. 2007.

[8] Toyama, et al. 2011. "A 17.7Mpixel 120fps CMOS Image Sensor with 34.8Gb/s Readout," IEEE ISSCC, 506–7.

[9] M. F. Snoeij et al., "Multiple-ramp column-parallel ADC architectures for CMOS image sensors," IEEE J. Solid-State Circuits, vol. 42, no. 12, pp. 2968–2967, Dec. 2007.

[10] Ham, Seogheon, Y. Lee, and W. Jung. 2006. "CMOS Image Sensor with Analog Gamma Correction Using Nonlinear Single-Slope ADC." 2006 IEEE International Symposium on Circuits and Systems. Ieee, 3578–81. ISCAS.2006

[11] T. Otaka, et al., "12-Bit Column-Parallel ADC with Accelerated Ramp", International Image Sensor Workshop (IISW) Karuizawa,, Japan, 2005.

[12] Y. Hwang, and M. Song. 2014. "Design of a CMOS Image Sensor Based on a 10-Bit Two-step Single-slope ADC," Journal of semiconductor technology and science, vol.14, (2014), 246–51.