DOI: 10.2352/ISSN.2470-1173.2016.12.IMSE-049

Design, implementation and evaluation of a TOF range image sensor using multi-tap lock-in pixels with cascaded charge draining and modulating gates

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Abstract

This paper presents the design, implementation and evaluation of a CMOS time-of-flight (TOF) range image sensor using multi-tap lock-in pixels controlled by cascaded charge draining and modulating gates. The proposed lock-in pixel is designed for reducing the power consumption of the TOF sensor chip and the dark current noise which arises from the multiple connections of floating diffusions, while ensuring the performance of high-speed charge transfer and preventing the influence of background light. The TOF range image sensor has 320(Column) x 240 (Row) effective pixels with the pixel size of 16.8μm x 16.8μm. The chip has been implemented using 0.11-μm 1-poly 4-metal CMOS image sensor process.

1. Introduction

A TOF range image sensor is an imaging device for measuring the distance of an object by Time-of-Flight (TOF) method. During the last several years, TOF range imagers using lock-in pixels have been developed and used for a wide variety of applications such as robotics, medicine, security, gesture recognition and gaming[1-2]. Numerous developments in the TOF technology have been reported, addressing many issues that affect the ability of TOF range image sensors and its solutions [3-7]. Pinned photodiode (PPD) is invented for noise reduction and high-speed charge transfer in the sensors. For compatibility to the main-stream image sensor technology, the TOF sensor pixel should be based on a standard pinned photodiode (PPD) based CMOS image sensor technology. However, because of the weak electric field modulation of the PPD by the transfer gates, the basic unit of the conventional PPD TOF pixels is designed with small dimension and plural of units are connected in parallel [7]. This type of design leads to large power consumption due to driving the large gate capacitance and large dark current of the charge accumulators [2]. In order to improve the performance of the range image sensors, this paper presents a CMOS TOF range image sensor based on multi-tap lock-in pixels with large-area high-speed photodiode and cascaded draining and modulating gates to minimize the generation of dark current while achieving high-speed charge transfer and capability of background light cancellation.

In lock-in pixel image sensors, high-speed charge transfer is essential. So far, in order to perform the high-speed transfer operation of charge carriers generated by the photodiode in the lock-in pixel, each pixel units are configured to be small, arranged in arrays and connected in parallel to each other. However, this increases the loading capacity of multiple transfer gate connected in parallel, and when the numbers of pixels becomes greater, the power consumption of the whole image sensor also increases. Besides, connecting numerous pixel units enlarges the area of the diffusion layer of the signal detection part, thus generating dark current in the sensor. To resolve these issues, we utilize a large-area photodiode instead of an array of sub-pixels in a pixel using a set of charge draining gates and multiple charge transfer gates. With this structure, the proposed pixel is able to reduce the dark current due to the decreasing number of floating diffusions.

2. Pixel structure and operation

The proposed CMOS TOF range image sensor using multi-tap lock-in pixels with large-area photodiode and cascaded draining and modulating gates is shown in Figure 1.

Pixel structure descriptions:

To transfer electric charge generated in the large-area photodiode to charge modulators in high speed, the n(n_1)-type doped layer of photodiode is designed in comb-shaped, thus electric charges can be collected in the central region of the photodiode. The n(n_2)-type layer is doped by double implantation in the channel region to conduct electric charges to the channel. There is a set of charge draining gates G_D sandwiching the channel region from both sides between photodiode and charge modulators. With this charge draining gate G_D, electric charge is controlled to be transferred to charge modulators or discharged to drain. Besides, charge modulators and the channel region extending from photodiode to charge modulators are shielded from incoming light. Therefore, the influence of background light can be reduced in the pixel. To realize time-of-flight measurement while canceling the background light, three charge transfer gates, namely G_1, G_2, and G_3, as shown in Figure 1, are used in this sensor.

Pixel operation:

When a middle voltage (1.5V) is applied to G_D, a potential barrier is formed to create channel in the potential diagram of X-X' cross sectional direction (Fg.2(a)). In this condition, there is no barrier formed in Y-Y' direction (Fg.2(b)) so that charge generated in the photodiode is transferred quickly to charge modulators. On the other hand, when a high voltage (3.3V) is applied to G_D, there is no potential barrier at X-X' direction, and charge at the channel is discharged to the drain. In this condition, as shown in the potential diagram of Y-Y' direction, the potential of the channel becomes higher than that of charge modulators and a dip is created on the channel, preventing electric charge to be transferred to charge modulators.

In the case of applying a middle voltage (1.5V) to G_D, by controlling the gate voltage of G_1, G_2 and G_3, accumulation operation to floating diffusions FD_1, FD_2 and FD_3 is possible. That is, when applying a low voltage (0V) to G_1, G_2 and a high voltage (3.3V) to G_3, charge is transferred to FD_3 as shown in Y-Y' direction. Then, when G_3 is in low voltage (0V), by applying 3.3V to G_1 and 0V to G_2, electric charge is transferred to FD_1 and vice versa as shown in X_1-X_1' direction (Fg.2(c)).

Figure 3 shows the timing diagram for background-cancelled TOF measurement of the sensor. FD_3 is accumulated by background light only while FD_1, FD_2 are used for accumulating signal charge.

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DOI: 10.2352/ISSN.2470-1173.2016.12.IMSE-049

With signal light pulse width T_0 and time of flight T_d, signal charge stored in FD_1, FD_2 and FD_3 are calculated as the following equations.

$$Q_1 = I_{ph}(T_0 - T_d) + I_a T_0 \quad (1)$$

$$Q_2 = I_{ph} T_d + I_a T_0 \quad (2)$$

$$Q_3 = I_a T_0 \quad (3)$$

where I_{ph}, I_a are photo current generated by signal light and background light, respectively. Hence, the time of flight is estimated as follow.

$$T_d = T_0 \frac{Q_2 - Q_3}{Q_1 + Q_2 - 2Q_3} \quad (4)$$

Finally, the range is calculated as

$$L = c\frac{T_d}{2} \quad (5)$$

where c is the light velocity ($c=3x10^8$ m/s).

3. Design and implementation of Lock-in pixels

Figure 4 shows the equivalent pixel circuits using active pixel type of readout circuits. The three signals are read out in parallel through column readout circuits. A prototype TOF imager has been implemented using a 0.11um standard CIS technology as shown in Figure 5. The total effective number of pixels is 320 x 240.

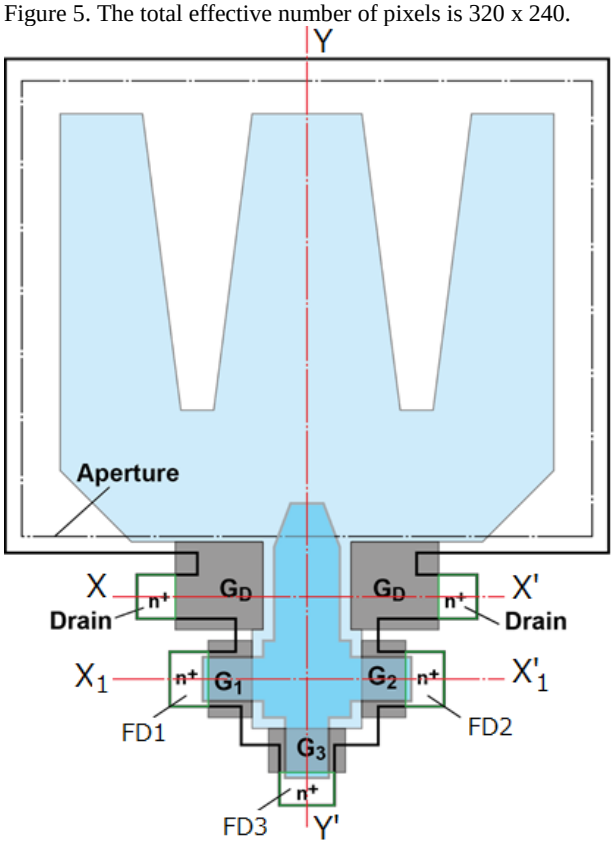
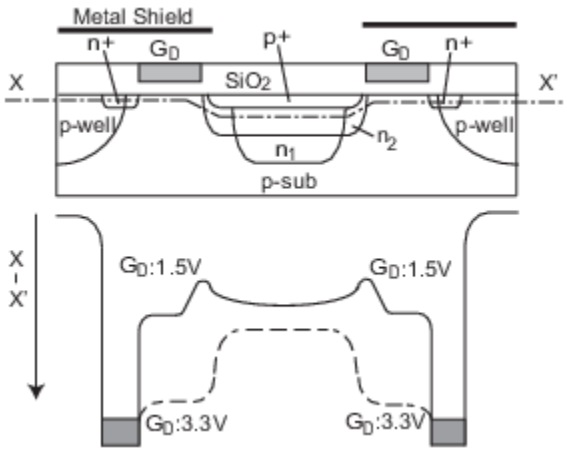
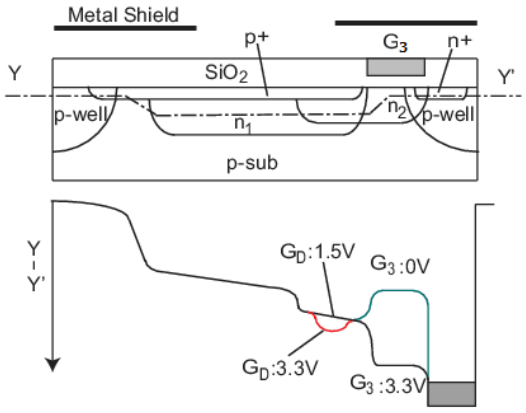


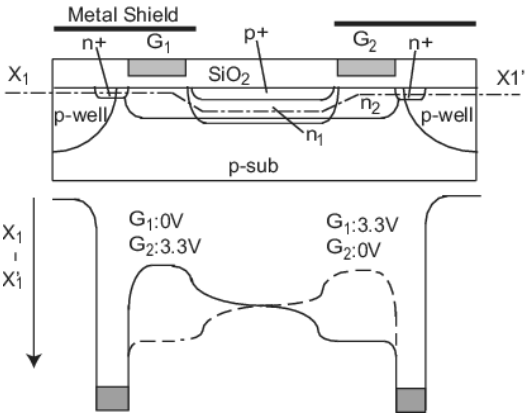
Figure 1. Pixel structure



(a). X-X' cross section



(b). Y-Y' cross section



(c) X_1-X_1' cross section

Figure 2. Potential diagram of cross sections

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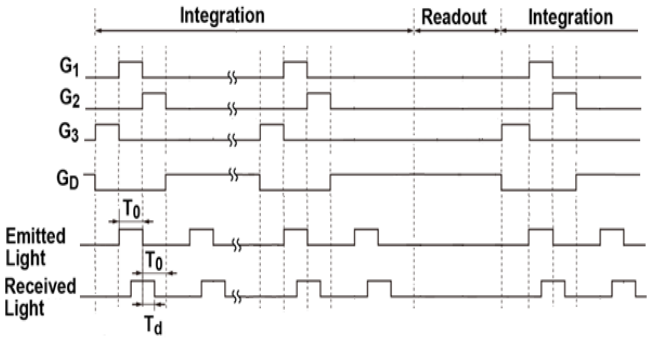


Figure 3. Timing diagram

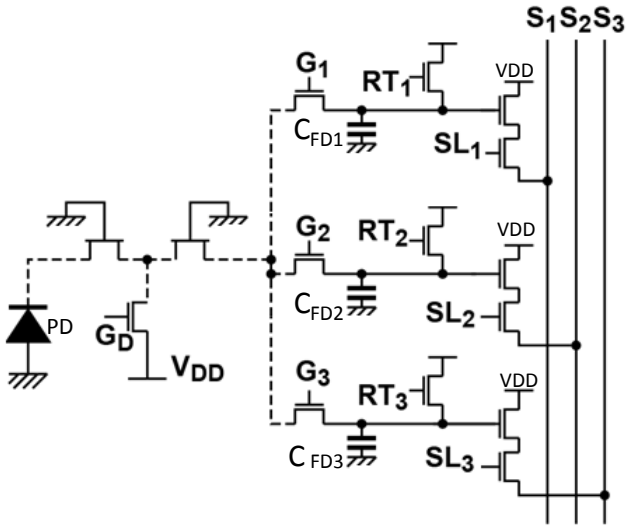


Figure 4. Pixel circuit schematic diagram

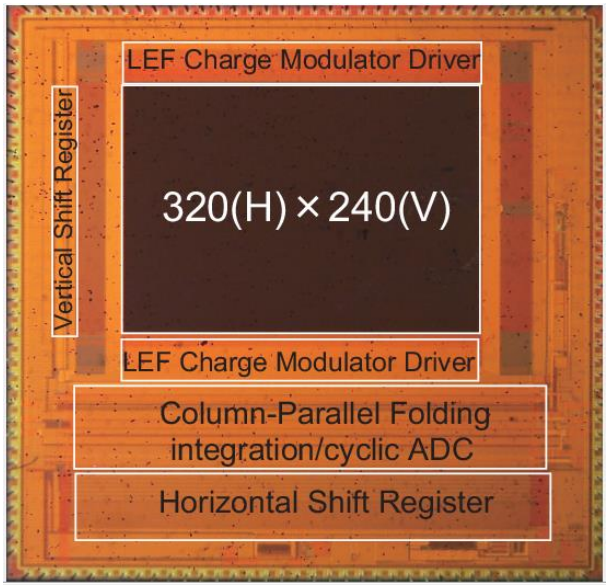
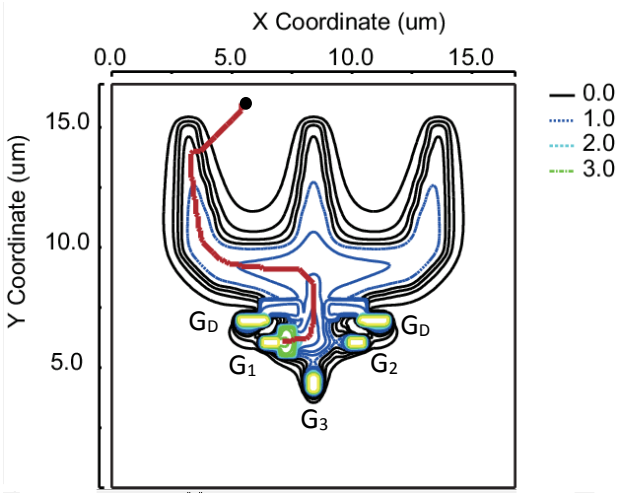


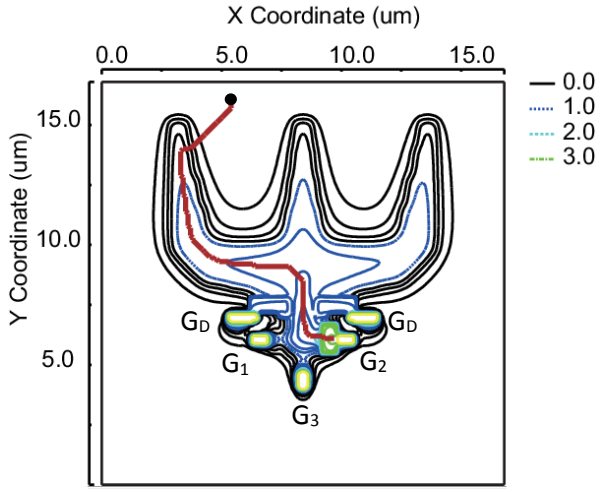
Figure 5. Sensor microphotograph

4. Simulation results

Figure 6 shows the simulation results of charge transfer behaviors of the proposed lock-in pixel. The black dot represents the initial position of charge before being transferred by electric field to drain and floating diffusions FD_1, FD_2 and FD_3, and the red line presents charge movement traces. As shown in simulation results, when one of the four gates G_1, G_2, G_3 and G_D is set to ON level and another three gates are set to OFF level, signal charge is transferred to the gate set to ON level. These simulation results indicate that the proposed lock-in pixel is working as intended.



(a) G_1: ON (3.3V), G_2, G_3: OFF (0V), G_D: OFF (1.5V)



(b) G_2: ON (3.3V), G_1, G_3: OFF (0V), G_D: OFF (1.5V)

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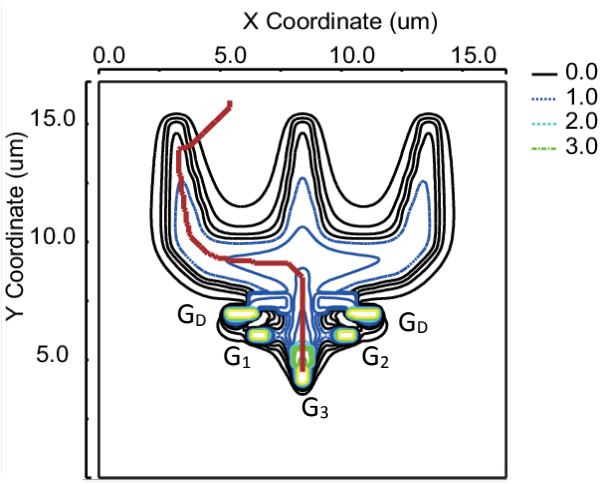
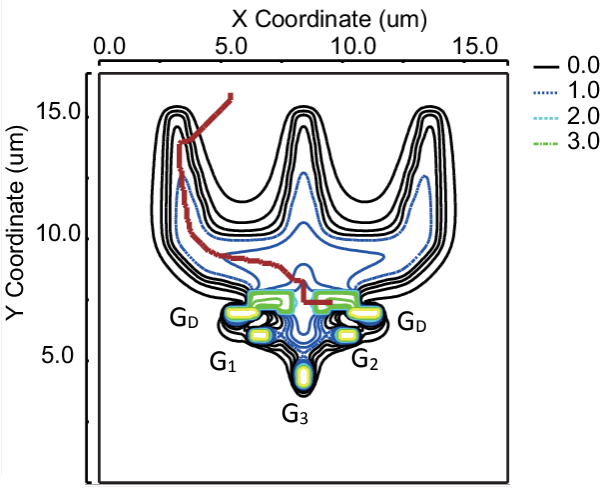


(c) G_3: ON (3.3V), G_1, G_2: OFF (0V), G_D: OFF (1.5V)



(d) G_D: ON (3.3V), G_1, G_2, G_3: OFF (0V)

Figure 6. Simulation results of charge transfer

5. Measurement results

Figure 7 shows measurement system for testing the proposed sensor. Test system includes a sensor board, a LED board and a data transmitter.

The experimental result of modulation characteristic shows the dependability of signal output to emitted light (LED) delay time as in Figure 9 (offset signal is set to be 0). The output signal of each gate increases when the signal charge of received light is stored successively to the activated gate and decreases when the signal charge of received light is stored successively to other gates that are activated (described as in Figure 8). Besides, dark current in the floating diffusions of the proposed sensor has been measured to be 5 mV/s at 24 degree Celsius, which is relatively small compared to other works.

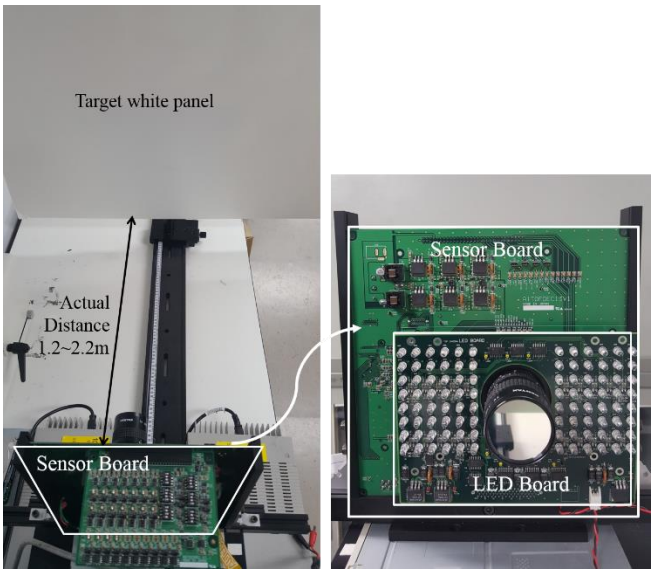


Figure 7. Measurement system

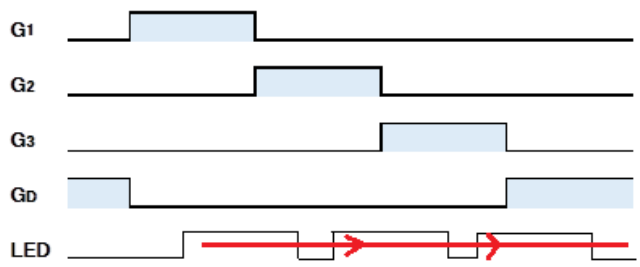


Figure 8. Delay timing diagram

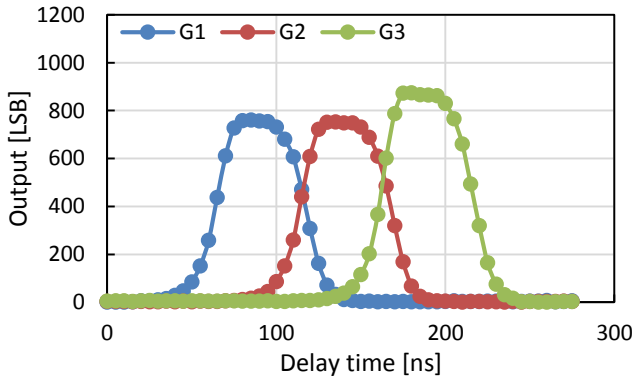


Figure 9. Modulation characteristic

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Figure 10 and 11 shows range linearity and range resolution of the proposed sensor under no background light condition, respectively. In range measurements, a flat white panel is used as an object and the distance from sensor to the flat white panel for the measurements is 1.2m to 2.2m. The measurements have been acquired with 30 frames considering a region of interest of 10x10 pixels. Figure 10 shows that the range has been correctly measured in the measured distance 1.2m ~ 2.2m and the maximum error between the measured distance and the actual distance can be suppressed to be approximately 2.5%.

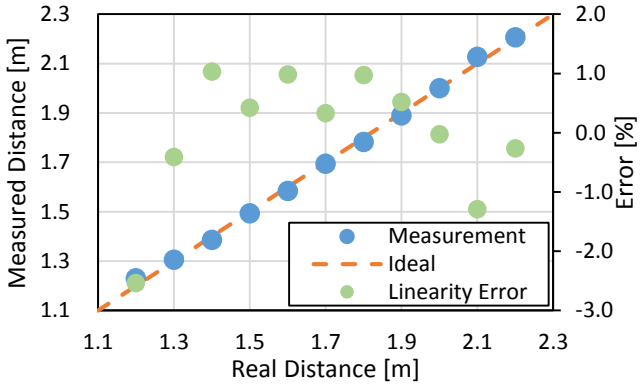

Figure 10. Range linearity and linearity error (after revision)

The range resolution shown in figure 11 under no background light condition is from 5cm to 20cm depending on the distance to be measured. The graph shows the range resolution has been derived by using the proposed sensor.

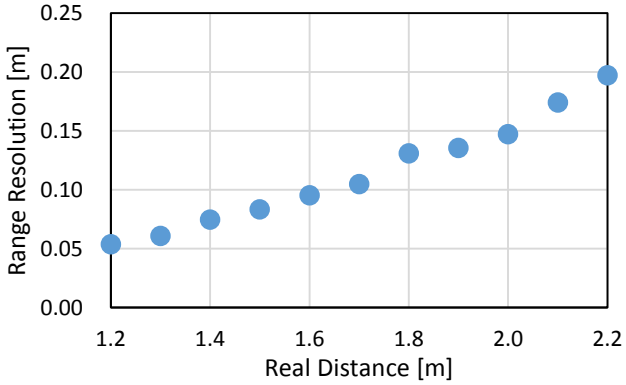

Figure 11. Range resolution (without background light)

Figure 12 shows linearity of intensity of G1, G2, G3 to a constant DC light as a basic characteristics of the sensor. Besides, photon transfer curve (PTC) for estimating conversion gain based on the linearity of intensity is shown in Figure 13. Data used to determine the conversion gain is the output of the G2. The resulting conversion gain is approximately 4.4μV/e$^-$.

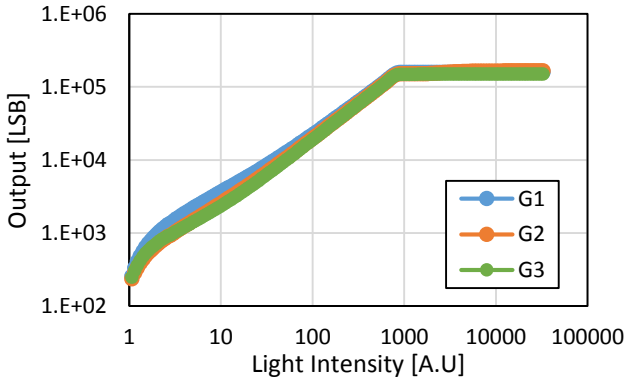

Figure 12. Linearity of intensity

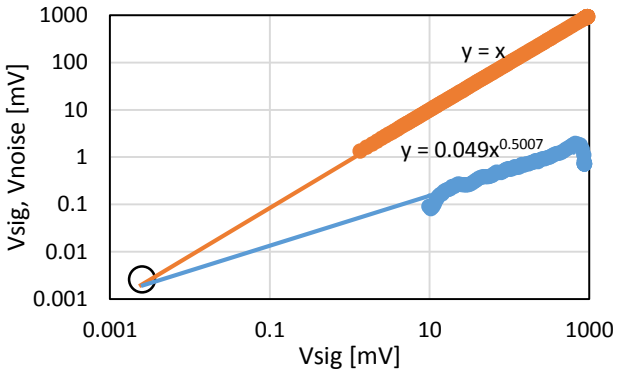

Figure 13. Photon transfer curve (PTC)

6. Conclusions

In this work, we utilized a large-area photodiode in a pixel instead of the conventional array of sub-pixels and charge modulation structure based on the cascading the draining and modulating gates. Since the number of floating diffusions is decreased, dark current generated in the floating diffusions are expected to be smaller than in conventional sensors. The reduced number of gates for charge modulation leads to low-power consumption of the chip. The reduced number of gates is also effective for driving high-speed modulating gates, which leads to better linearity or higher demodulation contrast of the TOF pixels. When compared with a similar pixel structure using double-polysilicon gates reported in [8], the proposed structure based on the pinned photodiode CMOS technology is better for low dark current, high-speed photo-carrier modulation and full-compatibility to the main-stream CMOS image sensor technology.

Acknowledgements

This work was partly supported by the JSPS Grant-in-Aid for Scientific Research (S), No. 25220905 and JST COI STREAM

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