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A CMOS image sensor with variable frame rate for low-power operation

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Abstract

In this paper, a complementary metal oxide semiconductor (CMOS) image sensor for low-power operation with a variable frame rate is presented. The operating current of the CIS can be reduced by varying the frame rate of the CMOS image sensor (CIS), thus decreasing power consumption effectively. The proposed image sensor has two modes: normal mode and low-power mode. In the low-power mode, the operating current of the pixel array can be controlled according to the frame rate of the CIS. At lower frame rates, the operating current of the pixel array is smaller than in the normal mode. The power consumption of the proposed CIS is determined by the on and off ratios of the bias current. The proposed image sensor was fabricated and measured with a 2-poly 4-metal 0.35 μm standard CMOS process.

1. Introduction

There is a sharply increasing demand for CMOS image sensors (CIS) in many applications such as mobile devices, digital single lens reflex (DSLR) cameras, and security cameras [1–3]. For this reason, various studies have focused on improving CIS performance. The key parameters of CIS performance are sensitivity, dynamic range, noise, and power consumption [4–9]. Among these parameters, power consumption is very important owing to the increasing use of mobile devices, and more studies on the reduction of power consumption are needed [10–12]. CIS technology requires scale reduction, higher resolution, and low noise, making low-power chip design difficult. There are already many low-power techniques for image sensors: energy harvesting, motion detection, block-based CISs, and so on. However, these technologies lead to poor image quality or require complex additional circuits for low-power operation [13–15].

In this study, we have developed a low-power CIS with a control function for the frame rate and the magnitude of the operating current. Because the frame rate of the CIS is proportional to its power consumption, the power consumption can be effectively decreased by reducing the frame rate. The image sensor has a bias circuit for the static current in the analog part. The total power of the image sensor decreases as the static current decreases. An additional simple circuit is used in the proposed image sensor to reduce the power consumption with a variable frame rate, while maintaining the quality of the image.

2. Operating principle

2.1 Method of variable frame rate

The frame rate is related to the exposure time in the conventional CIS. The exposure time is long when the frame rate is low because they are inversely related. In Figure 1–(a), many images are shown to be captured per unit time. The exposure time is short with a high frame rate. In the other method, shown in Figure 1–(b), the number of images captured per unit time is less than that with a high frame rate, and the exposure time is long with a low-frame rate. Accordingly, the brightness of the image, which is related to the exposure time, is changed by the frame rate. The total power of the image sensor is the same by the frame rate because the magnitude of the static current of the image sensor is the same per unit time in the conventional CIS.

The mechanism of the proposed image sensor is shown in Figure 1–(c). The power consumption can be reduced by repeating the on/off operation. The proposed image sensor has the same exposure time, and the static current does not flow continuously. For this reason, the power consumption is related to the frame on/off ratio in the image sensor.

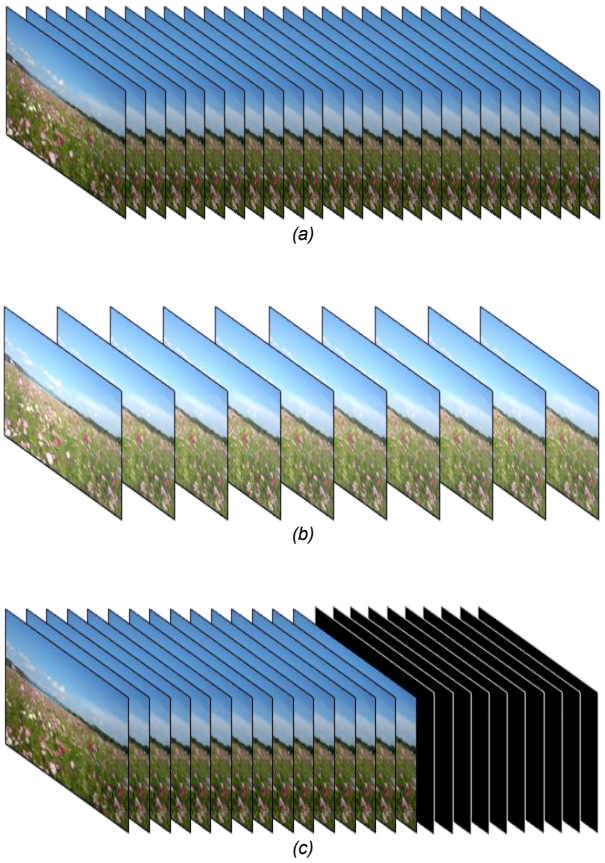

Figure 1. Expected images of the conventional image sensor with (a) high frame rate and (b) low frame rate. (c)The proposed image sensor with low frame rate.

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2.2 Architecture

The power sources of a chip are a pixel array, a bias circuit, driving circuits, and readout circuits. Among them, the pixel array and the bias circuit consume the most power in the image sensor. An active pixel sensor (APS) in the pixel array is composed of a p–n junction diode, transistors, and a source follower. The source follower requires a current mirror circuit to control the static current. The circuits related to the pixel bias part are shown in Figure 2, and the layout of the current mirror circuit is shown in Figure 3. The current mirror circuit comprises a resistor (R_1), a bias control circuit, and current mirrors. The magnitude of the current in a mirror circuit and pixel array can be controlled by R_1. The currents I_1, I_2, and I_{pixel} decrease with R_1. Further, it is possible to shut down the power per frame using the bias control circuit. The layout is implemented in a 0.35 µm conventional CMOS process.

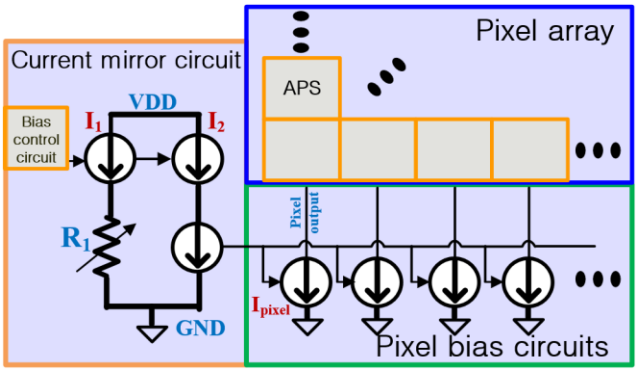

Figure 2. Schematic diagram of the pixel array, pixel bias circuit, and current mirror circuit.

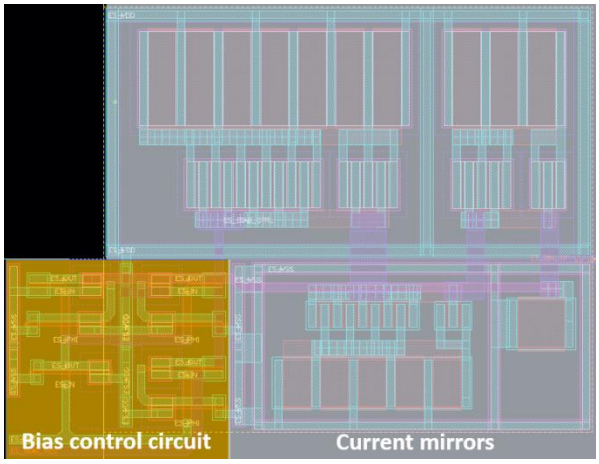

Figure 3. Layout of the proposed current mirror circuit.

Figure 4 shows a timing diagram with the power consumption of the proposed image sensor. There are two states in the proposed image sensor. In the ON state, the image sensor is operated with high power consumption. However, the image sensor is operated with low power consumption in the OFF state because the pixel bias circuits and the current mirrors are shut down. The image sensor has low and high frame rates as shown in Figures 2–(a) and 2–(b), respectively; the frame rate is related to the on/off ratio of the power. Accordingly, the power consumption decreases as the on/off ratio decreases, and the power consumption in the low-frame rate mode is reduced approximately 1/n times compared to the all-ON mode.

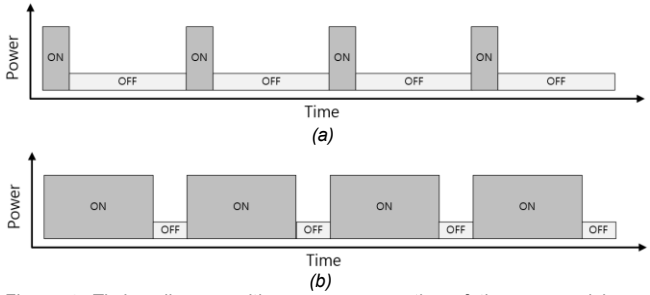

Figure 4. Timing diagram with power consumption of the proposed image sensor: (a) low-frame-rate mode, (b) high-frame-rate mode.

The layout of the proposed image sensor is shown in Figure 5. It is composed of a 170 × 210 pixel array, a driving circuit for the pixel array, a bias circuit, and column parallel readout circuits. The total size of the chip is 2.1 mm × 1.7 mm, the size of the APS is 8 µm × 8 µm, and its fill factor is 35%. The proposed image sensor was fabricated and measured using a standard CMOS 2-poly 4-metal 0.35 µm process.

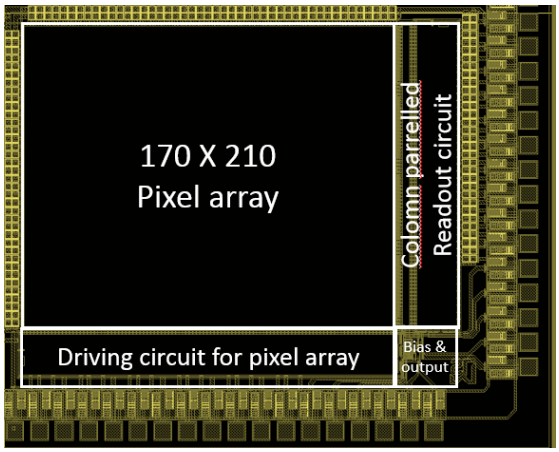

Figure 5. Layout of the proposed image sensor.

3. Measurement results

The measurement results showing the variation in the bias current with resistance is shown in Figure 6. I_1 decreases with R_1 in the current mirror circuit shown in Figure 2. The current and the power are proportional at 3.3 V supply voltage, and it is necessary to reduce the current for low-power operation without image degradation. The output image and the dynamic range when I_1 is varied are shown in Figure 7. The contrast of the image and the dynamic range are changed depending on I_1 because the output range of the APS and the magnitude of the noise are changed by I_1. The output image become darker with decreasing I_1, and the best result is obtained at 17 µA because the image sensor has the widest dynamic range at that current. A wide-dynamic-range image sensor can detect a wider range of scene illuminations and produce images with more detail.

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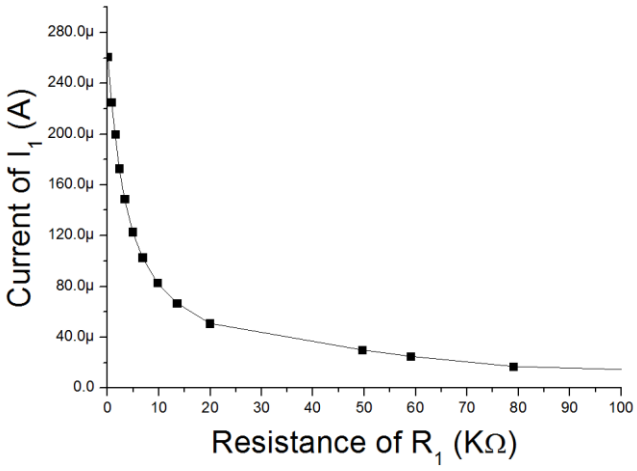


Figure 6. Measurement results showing variation of I_1 with R_1.

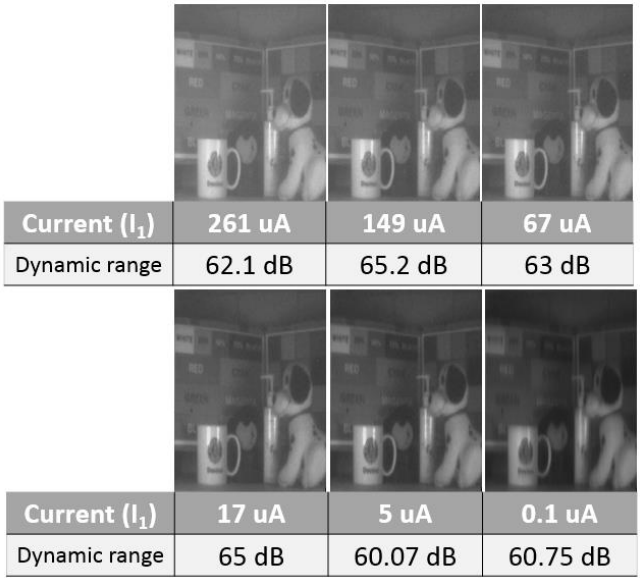


Figure 7. Output image and dynamic range for various values of the bias current.

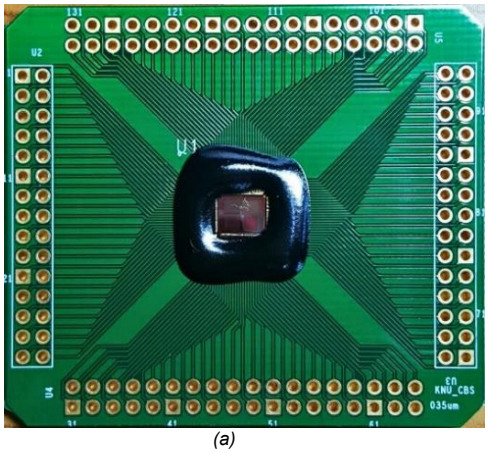
Figure 8 shows the total power consumption of the proposed image sensor with a variable frame rate. The power consumption is reduced to 0.161 mW/fps and is saved to 1.416 %/fps (frames per second). Even with a variable frame rate, the image quality is maintained, and the exposure time is fixed at 33 ms.

The current is 3.451 mA at the frame on state and 1.939 mA at the frame off state. A majority of the current is carried by the readout circuit and the bias circuit at the frame ON state, but it is carried by the readout circuit at the frame OFF state. The proposed image sensor exhibits a maximum power reduction of 35.41% at 5 frames per second.

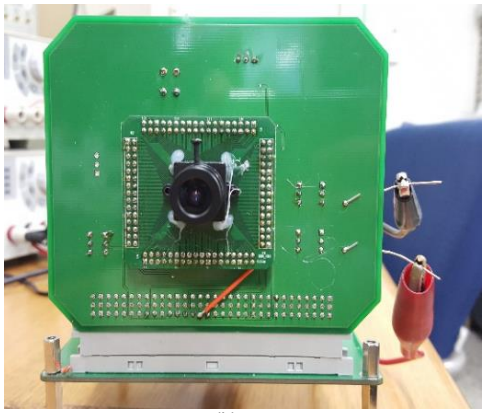
Frame rate (fps)	Total power (mW)	Power reduction(%)
5	7.356	35.41
10	8.135	28.57
15	8.936	21.53
20	9.778	14.14
25	10.600	6.93
30	11.388	0.00

Figure 8. Total power consumption of the proposed image sensor with variable frame rate.

A photograph of the printed circuit board (PCB) with a bonded chip is shown in Figure 9–(a), and Figure 9–(b) shows the image sensor system for the chip test. The camera lens is mounted on the PCB. The port of the PCB is connected to the field-programmable gate array (FPGA), and the control signal from the FPGA is applied to the port of the PCB. The overall performance characteristics of the proposed image sensor are summarized in Table 1.



(a)



(b)

Figure 9. Photographs of (a) the PCB with bonded chip and (b) the image sensor system for the chip test.

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Table 1. Characteristics of the proposed image sensor

Process	CMOS 2-poly 4-metal 0.35 μm
Supply voltage	3.3 V for analog and digital
Pixel size/fill factor	8 μm × 8 μm/35%
Resolution	170 × 210
Chip size	2.1 mm × 1.7 mm
Power	6.564–11.338 mW
Frame rate	5–30 fps

Discussion

In this paper, we propose a CIS with a variable frame rate for low-power operation. The proposed bias circuit can control the magnitude of the current in the mirror circuit and the current in the source follower in the pixel array. The proposed image sensor is operated at 30 frames per second for an exposure time of 33 ms. The total power consumption of the chip is 11.338 W. However, the total power consumption is reduced by 35.41% by lowering the frame rate. The proposed image sensor is fabricated and measured using a 0.35 μm standard CMOS process.

Acknowledgments

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